09/918 739

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David J. Corisis

Patent No.: 6,830,961 B2

Issued: December 14, 2004

For: METHODS FOR LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE

Attorney Docket No.: 2269-2811.5US
(96-0243.05/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

May 1, 2007 — Date

Signature

Leta M. Howard
Name (Type/Print)

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANT'S MISTAKES (37 C.F.R. § 1.323) AND PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
MAY 08 2007
of Correction

Sir:

It is noted that a combination of Applicant and Patent Office errors appear in this patent of a typographical nature or character and correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination. A certificate of correction in the form attached hereto is requested.

Please note that an Amendment Pursuant to 37 C.F.R. § 1.312(a) (copy enclosed) was filed concurrently with the issue fee on June 28, 2004, but was apparently not completely entered before issuance of the patent. Attached is a copy of the previously filed Amendment Pursuant to 37 C.F.R. § 1.312(a) and the date-stamped postcard, acknowledging receipt by the PTO, to provide proof of such filing. We have included subject matter of this amendment on the attached PTO/SB/44 with at least one copy being suitable for printing.

05/04/2007 AWONDAF1 00000043 6830961
01 FC:1811 100.00 OP

MAY - 8 2007

Please send the Certificate to:

Name: James R. Duzan
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

The fee of $100.00 as required by 37 C.F.R. § 1.20(a) is enclosed.

Attached hereto in duplicate is Form PTO/SB/44 with at least one copy being suitable for printing.

Respectfully submitted,

James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: May 1, 2007
JRD/csw

Enclosures: PTO/SB/44 in duplicate
Check No. 23692 in the amount of $100.00
Copy of Amendment Pursuant to 37 C.F.R. § 1.312(a)
Copy of date-stamped postcard
Document in ProLaw

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,830,961 B2
DATED : December 14, 2004
INVENTOR(S) : David J. Corisis

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the specification:

COLUMN 4,	LINE 63,	change "the first" to --the second--
COLUMN 5,	LINE 24,	change "semiconductor **200**" to --semiconductor **100**--
COLUMN 6,	LINE 34,	change "the first plurality" to --the second plurality--
COLUMN 7,	LINE 51,	change "the first plurality" to --the second plurality--

In the claims:

CLAIM 1	COLUMN 9,	LINE 4,	change "a the" to --of the--
CLAIM 1	COLUMN 9,	LINE 12,	change "adjacent a" to --adjacent the--
CLAIM 4	COLUMN 9,	LINE 25,	change "including the step of:" to --including:--
CLAIM 5	COLUMN 9,	LINE 27,	change "including the step of:" to --including:--
CLAIM 9	COLUMN 10,	LINE 7,	change "an end" to --the end--
CLAIM 10	COLUMN 10,	LINE 9,	change "the at least one" to --each--
CLAIM 11	COLUMN 10,	LINE 20,	change "an end" to --the end--
CLAIM 11	COLUMN 10,	LINE 22,	change "beyond a" to --beyond the--
CLAIM 12	COLUMN 10,	LINE 29,	change "an end" to --the end--
CLAIM 12	COLUMN 10,	LINE 31,	change "an end" to --the end--
CLAIM 12	COLUMN 10,	LINE 34,	change "beyond a" to --beyond the--

MAILING ADDRESS OF SENDER:

PATENT NO. 6,830,961 B2

James R. Duzan
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

No. of additional copies

MAY - 8 2007

THE P[illegible]NT & TRADEMARK OFFICE MAILROOM DA[illegible] STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Letter; Part B-Issue Fee Transmittal; Amendment under 37 C.F.R. § 1.312(a); Copy of FIG. 1 with changes made in red; Replacement Formal Drawing FIG. 1; Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees.

Invention:	METHODS FOR LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE
Applicant(s):	David J. Corisis
Filing Date:	July 31, 2001
Serial No.:	09/918,739
Date Sent:	June 28, 2004 via first class mail
Docket No.:	2269-2811.5US
JRD/dp	

MAY - 8 2007

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: David J. Corisis

Serial No.: 09/918,739

Filed: July 31, 2001

For: METHODS FOR LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE

Confirmation No.: 3239

Examiner: D. Graybill

Group Art Unit: 2827

Attorney Docket No.: 2269-2811.5US
(96-0243.05/US)

Notice of Allowance Mailed:

March 30, 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 28, 2004
Date

Signature

Deidra J. Pfeil
Name (Type/Print)

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Specification appear on page 2 of this paper.

A **Listing of the Claims** begins on page 3 of this paper.

Amendments to the Drawings appear on page 6 of this paper and include both attached replacement sheet and annotated sheet showing changes.

Remarks begin on page 7 of this paper.

IN THE SPECIFICATION:

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] United States Patent 4,862,245 to Pashby illustrates a "leads-over-chip" (LOC) configuration, wherein the inner lead ends of a standard dual-in-line package (DIP) lead frame configuration extend over and are secured to the active (upper) surface of the semiconductor device through a dielectric layer. The bond wire length is shortened by placing the inner lead ends in closer proximity to a central row of die bond pads, and the lead extensions purportedly enhance heat transfer from the semiconductor device. However, the Pashby LOC configuration, as disclosed, relates to mounting and bonding a single semiconductor device with the inner lead ends of the lead fingers to the surface of the semiconductor device.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] Fig. 2 is a ~~cross-sectional~~ cross-sectional view taken along line A-A of Fig. 1 of a portion of the semiconductor assembly of the first embodiment of the present invention;

IN THE CLAIMS:

Claims 1 through 19 were previously cancelled. None of the claims have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

Listing of Claims:

1.-19. (Cancelled)

20. (Previously presented) A manufacturing method for a lead frame for a semiconductor assembly having a semiconductor device having two opposed peripheral sides, two opposed ends, an active surface in a first horizontal plane, a bottom inactive surface in a second horizontal plane, and a plurality of bond pads located on the active surface of the semiconductor device, a first portion of the plurality of bond pads located adjacent one of the two opposed peripheral sides and a second portion of the plurality of bond pads located adjacent another of the two opposed peripheral sides, said method comprising:

forming a first plurality of lead fingers extending substantially in the first horizontal plane of the active surface of the semiconductor device, each lead finger of the first plurality of lead fingers terminating in an end located adjacent a peripheral side of the two opposed peripheral sides of the semiconductor device;

forming a second plurality of lead fingers having portions thereof extending below the bottom inactive surface of the semiconductor device and having portions thereof extending in the first horizontal plane of said active surface of said semiconductor device, said second plurality of lead fingers having portions extending substantially inwardly and extending downwardly from said first horizontal plane of the active surface of the semiconductor device placing portions of said lead fingers in a second substantially horizontal plane for providing support surfaces for portions of said inactive surface of said semiconductor

device, each lead finger of the second plurality of lead fingers having a portion thereof extending adjacent an end of the two opposed ends of the semiconductor device and terminating in an end located adjacent the peripheral side of the two opposed peripheral sides of the semiconductor device, at least one lead finger of the second plurality of lead fingers including a section extending substantially in the first horizontal plane; and

forming a die paddle for attaching portions of said inactive surface of said semiconductor device.

21. (Original) The method of claim 20, wherein the ends of the first plurality of lead fingers extend past the ends of adjacent lead fingers of the second plurality of lead fingers.

22. (Original) The method of claim 20, wherein the ends of the second plurality of lead fingers extend past the ends of adjacent lead fingers of the first plurality of lead fingers.

23. (Previously presented) The method of claim 20, further including:

placing tape on the second plurality of lead fingers.

24. (Previously presented) The method of claim 20, further including:

placing tape between the die paddle and the bottom inactive surface of the semiconductor device.

25. (Original) The method of claim 20, further including:

placing tape between the die paddle and the second plurality of lead fingers and the bottom inactive surface of the semiconductor device.

26. (Original) The method of claim 24, further comprising:

adhesively attaching the second plurality of lead fingers to the tape.

27. (Original) The method of claim 26, further comprising:

adhesively attaching the second plurality of lead fingers to the tape using thermosetting adhesive.

28. (Previously presented) The method of claim 20, wherein the die paddle includes at least one portion thereon extending beyond the peripheral side of the two opposed peripheral sides and at least another portion thereof extending beyond the end of the two opposed ends of the semiconductor device.

29. (Previously presented) The method of claim 20, wherein each lead finger of the second plurality of lead fingers includes an offset therein.

30. (Previously presented) The method of claim 20, wherein the second plurality of lead fingers includes:

at least one lead finger having a portion thereof extending adjacent a portion of a lead finger of the first plurality of lead fingers, a portion thereof extending substantially adjacent the end of the two opposed ends of the semiconductor device, a portion extending substantially opposed to the end of the two opposed ends of the semiconductor device, and having a portion extending beyond the peripheral side of the two opposed peripheral sides of the semiconductor device.

31. (Previously presented) The method of claim 20, wherein the second plurality of lead fingers includes:

at least one lead finger having a portion thereof extending adjacent a portion of a lead finger of the first plurality of lead fingers, a portion thereof extending substantially adjacent the end of the two opposed ends of the semiconductor device, a portion extending substantially opposed to the end of the opposed ends of the semiconductor device and extending adjacent a portion of the die paddle, and having a portion extending beyond the peripheral side of the two opposed peripheral sides of the semiconductor device.

IN THE DRAWINGS:

The attached drawing sheet includes changes to FIG. 1. This sheet replaces the original FIG. 1.

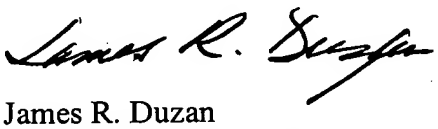
Specifically, FIG. 1 has been revised to delete both occurrences of reference numeral "16" with appropriate lead lines. No new matter has been added.

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,



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Date: June 28, 2004
JRD/csw

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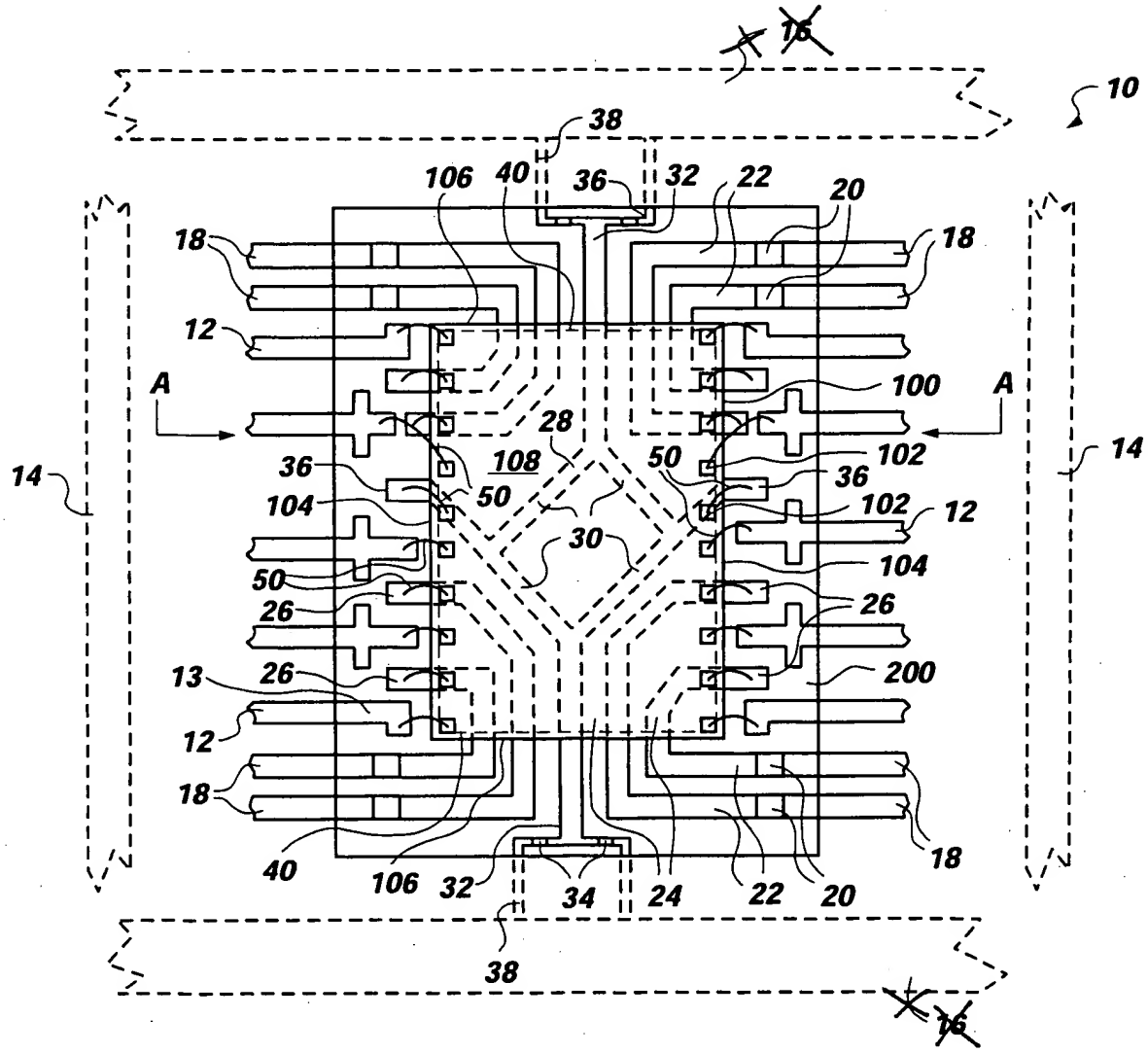

Fig. 1

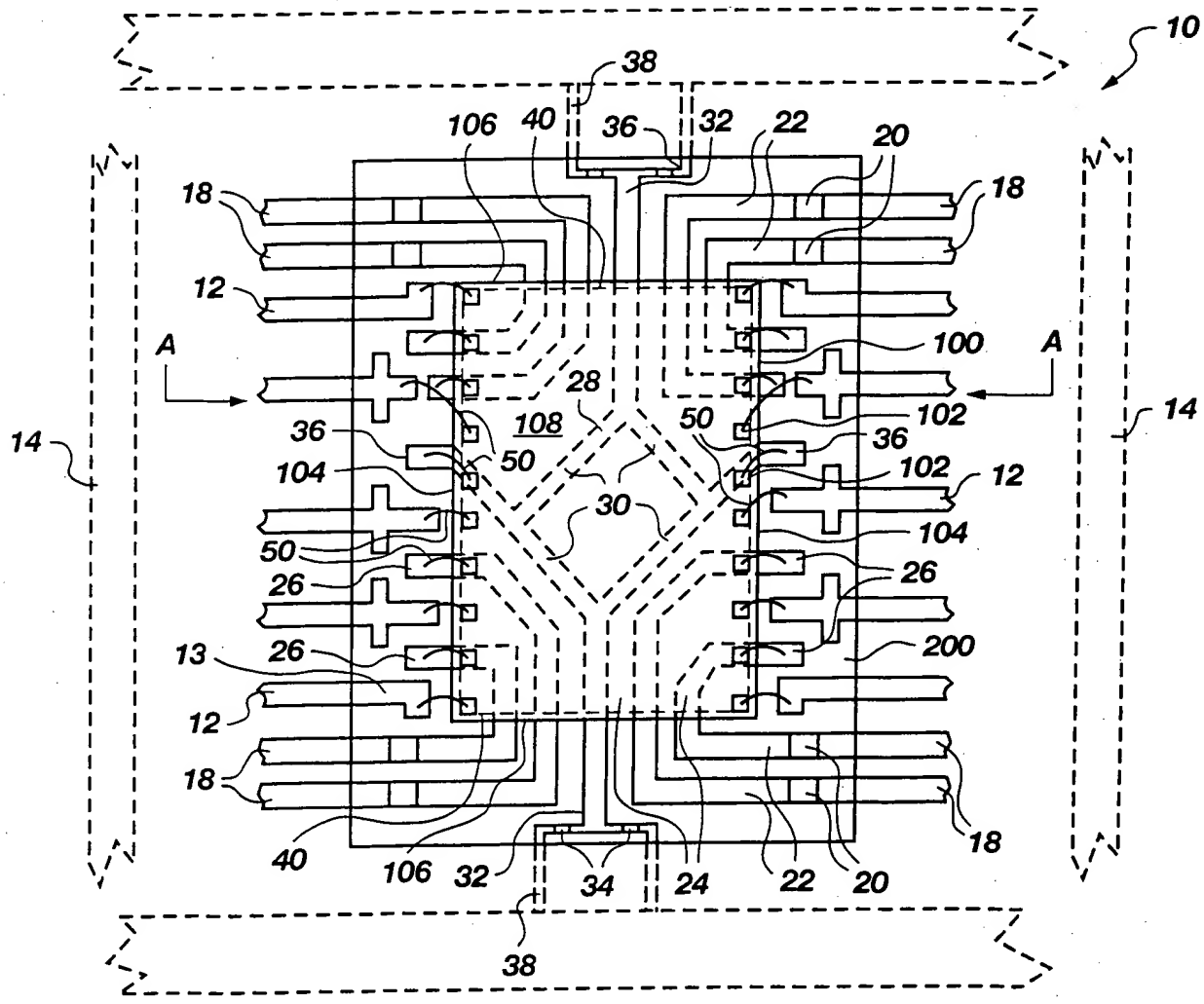

Fig. 1